AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

1. **(Currently Amended)** In a system that asserts a false synchronization signal at times when data is not present, a fiber-optic transponder that produces a lock signal only when data is present in a serial data signal, the transponder comprising:

a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode, wherein the phase locked loop is further adapted to assert a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency and wherein the phase locked loop is further adapted to keep the synchronization signal asserted as long as the phase locked loop is locked onto the serial data signal; [[and]]

a timing circuit adapted to measure a period of time that the synchronization signal is asserted using a capacitor and resistor network and to produce a lock signal if the synchronization signal is asserted for at least a specified period of time[[;]], the timing circuit including a comparator that compares a first reference signal with a signal from the capacitor and resistor network used to measure the period of time that the synchronization signal is asserted, the comparator outputting the lock signal based on the comparison; and

a demultiplexer arranged to receive a clock signal from the phase locked loop, the demultiplexer being configured to convert the serial data signal to a parallel data signal based on the clock signal.

2. **(Canceled)**

3. **(Currently Amended)** The transponder of claim 1,[[2,]] wherein the timing circuit comprises a transistor for resetting the timing circuit.

4. **(Previously Presented)** The transponder of claim 3, wherein the transistor is at least one of a field effect transistor, a PNP bipolar junction transistor, and NPN bipolar junction transistor.

5. **(Cancelled)**

6. **(Currently Amended)** The transponder of claim 1, further comprising an input level detector that compares the synchronization signal with a second reference signal and produces logical signals that are fed into the timing circuit.

7. **(Currently Amended)** The transponder of claim [[2,]]1, wherein the timing circuit ~~further comprising a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that~~ outputs the lock signal to a host device ~~based on the value of the reference signal compared to the signal from the capacitor and resistor network~~.

8. **(Original)** The transponder of claim 7, wherein the comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value.

9. **(Currently Amended)** A fiber-optic transponder comprising:

an output adapted to couple to a host device;

a controller chip having a phase locked loop that is adapted to operate in a hunting mode in which the phase locked loop briefly asserts a synchronization signal when a hunting frequency passes through a data signal frequency that corresponds to a rate of data encoded in a data signal, the phase locked loop also being adapted to operate in a locked mode in which the phase locked loop asserts the synchronization signal so long as the phase locked loop is locked onto the data signal; and

a translation circuit including:

a level detector that compares the synchronization signal with a first reference signal to produce a logical signal based on the comparison;

a timer adapted to measure a period of time that the logical signal is asserted to produce a timer signal; and

a comparator that compares the timer signal with a second reference signal to produce a lock signal for use by the host device,

~~adapted to convert the synchronization signal from the controller chip to a lock signal usable by the host device,~~ wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal for the period of time measured by the timer and is de-asserted when the phase locked loop asserts the synchronization signal in hunting mode.

10.-12. **(Canceled)**

13. **(Currently Amended)** The fiber-optic transponder of claim 9,[[12,]] wherein the comparator includes feedback that changes a logical level of the lock signal when the value of the lock signal changes by some value greater than a hysteresis threshold value.

14. **(Currently Amended)** A method of mediating signals from a controller chip used in a fiber-optic transponder with a host device, the method comprising:

receiving a ~~an asserted~~ synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip;

obtaining an average of the synchronization signal over a period of time;

comparing the average of the synchronization signal with a reference signal to determine ~~determining~~ whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency;

asserting a lock signal if the phase locked loop has locked onto the data signal; and

in response to the asserted lock signal:

sampling data from the data signal;

extracting a clock signal from the data signal; and

using the extracted clock signal as a reference for converting the sampled data into synchronized data to be read by the host device.

15.-17. **(Canceled)**

18. **(Original)** The method of claim 14, further comprising changing a logical level of the lock signal when the value of the lock signal changes by some value greater than a hysteresis threshold value.

19. **(Previously Presented)** In a system that generates a synchronization signal to indicate the presence of a data signal, a translation circuit comprising:

a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted, wherein the timing circuit is further adapted to generate an output signal having a voltage across the capacitor; and

a comparator circuit adapted to compare the output signal with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time.

20. **(Original)** The translation circuit of claim 19, wherein the timing circuit comprises a transistor that is controlled by the synchronization signal for resetting the timing circuit such that the capacitor discharges.

21. **(Original)** The translation circuit of claim 20, wherein the transistor is at least one of a PNP bipolar junction transistor, an NPN bipolar junction transistor, and a field effect transistor.

22. **(Original)** The translation circuit of claim 19, wherein the comparator circuit includes feedback that changes a logical level of the lock signal useful by the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value of the comparator circuit.

23. **(Original)** The translation circuit of claim 22, wherein the hysteresis threshold value of the comparator circuit prevents the lock signal from changing logic levels until the output signal of the timing circuit changes by an amount greater than the hysteresis threshold value.

24. **(Original)** The translation circuit of claim 22, further comprising an input level detector that passes the synchronization signal to the timing circuit when the synchronization signal exceeds a reference voltage.

25. **(Cancelled)**

26. **(Previously Presented)** The translation circuit of claim 20 wherein the capacitor is coupled to the transistor such that current flows through the transistor to charge the capacitor when the synchronization signal is not asserted at a rate faster than a rate at which the capacitor discharges through a resistor coupled thereto, and wherein the comparator is adapted to assert the lock signal when the reference signal exceeds the voltage across the capacitor.

27. **(Previously Presented)** The fiber-optic transponder of claim 9, wherein the data signal is an electronic data signal, the fiber-optic transponder further comprising circuitry to convert an optical data signal to the electronic data signal.

28. **(Previously Presented)** The translation circuit of claim 19, wherein the capacitor is arranged such that a voltage across the capacitor is an average of the synchronization signal over a period of time.

29. **(Previously Presented)** The fiber-optic transponder of claim 9, wherein the data encoded in the data signal is digital data encoded with data encoding circuitry.

30. **(New)** The method of claim 14, wherein obtaining the average includes creating a time lag between when a change occurs in the synchronization signal and when the change is taken into account by the average of the synchronization signal.